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Centre de Physique des Particules de Marseille

CNRS - IN2P3 - Université Aix-Marseille II

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163, Avenue de Luminy - Case 907
13288 MARSEILLE CEDEX 9 - FRANCE

A Pixel Detector for the '95 Upgrade of the DELPHI MicroVertex Detector

D. SAUVAGE [1], J.C. CLEMENS, M. COHEN-SOLAL, M. RAYMOND, P.A. DELPIERRE

Centre de Physique des Particules de Marseille - IN2P3 - CNRS
Université d'Aix-Marseille II, Luminy, Case 907,
F-13288 Marseille Cedex 9, France

This work is a joint effort of the Delphi VFT Pixel Group [2]

Abstract

Silicon pixel diodes have been proposed as an upgrade detector for the DELPHI MVD, to be installed at the beginning of 1996, for the starting of LEP200. A total area of 1300 cm^2, read out by true 2D sparsing on-chip electronics, will cover the forward region, down to 12°. The detector and the readout chip will be described. The very peculiar aspect of interconnection and packaging will be presented. Also, early beam tests with fully equipped modules, will be reported, and future prospects will be addressed.

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[1] sauvage@cppm.in2p3.fr

[2] IN2P3/ISN, Grenoble; Institut für Exp. Kernphysik, Karlsruhe; IN2P3/C.P.P.Marseille; INFN/Univ. di Milano; IN2P3/CdF/LPC, Paris; FZU/Inst. of Physics, Praha; Bergische Universität, Wuppertal.

1 Introduction

Silicon strip detectors have shown their huge capabilities for several aspects of high energy physics instrumentation. However, with the ever increasing luminosity of accelerators, the demand for accurate, fast and unambiguous track reconstruction, for example, is also growing and silicon strips do have some limits, even when double-sided detectors are used. The pixel detector is presently the best answer to solve most of these limiting factors. While several planes of such modules are already taking data within WA97 [1], a full detector has been proposed, and is under construction, to improve the performance of the DELPHI MVD in the very forward region [2]. This challenging detector will improve the pattern recognition capabilities, e.g. for 4-jet event tagging, and help for particle identification, with momentum measurement in front of the forward RICH detectors (Fig. 1).

To extend the angular coverage of the existing detector, endcaps have been added (Fig. 2), of which two layers out of 4, are made of pixels. The pixel layers are located where the space constraint is the most severe. The other two layers are made out of ministrip detectors, glued back to back to provide two-coordinate projective readout [3]. Pixel detectors suit very well the space requirement in the sense that the full geometrical area covered by the detector is made of sensitive material, with the electronics sitting on the detector itself (see chapter 2). Also, while it is geometrically difficult (and costly as far as material thickness is concerned) to tile a cone with rectangular modules, as it is mostly the case with strips, the pixel option allows to design petal-shaped modules in an easy and convenient way; the only constraint being to have electronic chips of two sizes (in our case), one of 24×24 cells, and the other of 16×24 cells (Fig. 3).

2 A detector module: the hybride technique

Pixel detectors are being studied and developped over the world using two approaches: the monolithic one (where the detector and its electronics are implanted on the same piece of silicon), and the hybrid one (where the electronics sits on a different chip, on top of the detector (fig. 4)). Because we obviously want to built detector modules of rather large sizes, and for other important reasons like tests, detector price or chip interconnections layout,

we chose the hybrid technique. With this option, we can have a detector as large as what we are used to for a standard strip detector, at a reasonnable cost and yield. On the electronic side, the chip size is limited by the reticle size, which is a true geometrical constraint, and by the yield per wafer, which is process-related. A compromise has to be found, taking into account the cost of production for extra wafers, for example. Furthermore, as developped in the next chapter, the hybrid choice has the another advantage to allow the choice of the best chip sorting and matching to build each module.

A quite novel aspect of packaging, for the construction of the modules, is also the fact that no extra support has been added to the module. Because material thickness is of prime concern in this region of the detector, we have not used a ceramic circuit underneath the detector to route the bus and power lines that connect all the chips. We have made a MCM (multichip module), where the substrate is active, and acts as the mechanical structure, which is quite new in the hybrid microelectronics field. To do this, a double-metal process, as proposed by our detector founder, was improved (in terms of yield, interstrip capacitance, and line resistance) and used to route a bus connecting the 8 chips on each side of the module. When necessary, the electronic chip I/O signals were fed through tri-state registers, allowing multiplexing on the bus, and a reduction in the amount of signals by a factor greater than 6.

3 The readout electronics

As far as electronics is concerned, pixel detectors introduce some advantages, but also some contraints. Pixel capacitance is smaller, which has incidence on the power consumption and on the signal-to-noise performance. On the other hand, the available area to implement the electronics cannot be larger than the cell size required by the physics. Also the contact pad has to be included on the same area. Crosstalk is a major concern, as several hundreds of identical cells are duplicated to build up the 2D array. Finally, to be able to tile as many chips as possible on a single detector module, all the I/O pads have to be layed out only on one side of the chip, so that the approach distance between adjacent chips, as well as the dead space on the detector, can be minimized for the other 3 sides. The discussion on electronics naturally splits in 2 parts : the analog chain, and the digital processing and readout stage.

The front-end (analog) part of the circuit has been developped previ-

ously, mostly within the framework of RD19, at CERN [4]. It consists of a preamplifier, a shaping discriminator, followed by a comparator and a one-bit (D-latch) memory. The amplifier input transistor has been modified to match the larger bonding pad capacitance, and a gate was added, which will be opened only at beam cross-over (b.c.o.) time [5].

Several internal chip parameters can be tuned by adjusting externally 4 current polarisations. However, with these currents set to nominal values, different chips troughout a same wafer will exhibit different behaviours, especially in the preamplifier shaping and gain, and for the discriminator threshold. Because 8 chips are connected together on the integrated readout bus, special care must be taken to match these characteristics. Hence, we have developped an automatic test procedure. A full undiced wafer is scanned twice : once to look for general features of the chip behaviour, basic satisfactory functionning (in digital mode), and average values for the various polarisations. Then, during a second pass, detailed dependance of selected sensitive parameters is recorded. The chips can then be represented in a scatter plot, the axes being the slope-of-the-threshold vs. the threshold. From that, we finally extract groups of 16 well-matched circuits (the good success of this selection procedure can be seen in Fig. 9; see in chapter 5 : Beam test results).

Because of the large amount of pixels (over 1.2 million) to be read, a selective readout scheme was implemented. As only few hundreds pixels are hit per b.c.o., it is worthwhile to skip all the other pixels, using a zero-suppression-like technique. We call this technique Sparse Data Scan [6] (SDS) (Fig. 5). The matrix is scanned by a priority encoding circuit, first by line, then by column within a line. When a pixel is hit, a first switch is closed, that signals to the end of the corresponding line that this line contains a hit, while a second switch shorts an x-y bus inside the pixel matrix. At readout, an asynchronous signal runs through the lines, until it finds the first hit line. While this line number is decoded and buffered as a 5-bit word, the same signal propagates to the corresponding column, through the hit pixel, allowing the column number to be decoded as well. The non-hit columns are skipped, and when the line is read, it is automatically reset, and the priority is transmitted to the next hit line.

4 Packaging overview

Because the size of the sensitive cell is relatively large, the connecting element to the electronic chain can also be rather large (150μm). Our experience within RD19 being that a conventional flip-chip technique could be rather expensive, a special effort was devoted to this point and several "cheap" techniques have been investigated by members of the collaboration, in order to produce modules at an attracting cost, but also to provide fast and low-cost prototyping at the laboratory level, and chip evaluation, where the connection to the detector is essential to validate the readout response.

Our colleagues from INFN Milano have concentrated in conductive glue deposition by the screen printing technique.

We, at CPPM, have developped a technique based on anisotropic conductive adhesives. It is used in portable appliances, for connectorless connections between LCD displays, flex kapton cables and/or motherboard PCBs (Fig. 6), and has been tested for passive connections in microstrips detectors [7]. One advantage of this method, besides its low price, is the fact that the connecting media is provided as a stabilized film/tape of some insulating polymer, including small grains of conducting material. When the tape has been shaped to size and sandwiched between the detector and the chip, a thermo-compression process is used to melt the polymer, and put into electrical contact the two opposite pads, with the help of the metallic grains. While this is made easier when one of the two "circuits" is soft, the whole difficulty was to make this process work for a rigid-to-rigid connection.

Good contact resistance and repeatibility ($\sim$ 200mΩ, over several hundreds of contacts) have been achieved with this second technique. Some success has been achieved with the conductive glue process, while some basic problems are still under study. Unfortunately, the yield when connecting 16 chips to a single bus, including all the I/O pads, has not allowed for using these solutions in the construction of the final detector. A more industrial and proven solution was chosen, the C4 (controlled collapse chip connection) process (Fig. 7). This is a 20-year old IBM patent, mostly dedicated to internal production, but recently released to the public market, and much cheaper than previously used processes. Several modules have been already successfully built by this manufacturer and steps are being taken to set up the procedure for mass production.

5 Beam test results

Extensive tests have been performed in the laboratory, using calibration signals and a radioactive ^{90}Sr source.

However, in order to measure the detector efficiency, as well as the track reconstruction capability, we have tested several single- and multi-chip modules in beam, at CERN. A full module detector was installed in a 100 GeV pion beam, last June, and tracks were reconstructed using a 4-plane microstrip telescope. The full module was scanned in two positions, perpendicular to the beam, and at 40°, which represents the worst situation when the detector is installed in DELPHI.

Measured efficiency for the 16 chips, is presented in Fig. 8, as a function of the applied threshold. A good agreement is seen with a Monte Carlo simulation including the charge sharing between adjacent pixels (it should be noted that at that time, the chip matching procedure was not optimized, which causes some differences of response between several chips on the same bus; the situation has improved since, as shown in Fig. 9, which represents a source scan of a "matched" module).

The detector resolution is shown in Fig. 10, plotted as a function of the discriminator threshold. In the case of digital readout, with perpendicular tracks well inside the pixel, the expected resolution is equal to the pitch, divided by $\sqrt{12}$. These is clearly the case in the y direction. For the x direction, because we use data from the run where our module was tilted within respect to the beam axis, this resolution is much improved by the enhanced charge sharing, due to this tilt.

6 Conclusions and future prospects

The decision to install pixel detectors in the LEP200 version of the DELPHI experiment, demonstrates the maturity of this new technique. Major advances have been made in electronics designs, interconnection and module packaging, and detector integration. The proposed planning for the construction of the VFT assumes that we will install this detector as planned at the next LEP shutdown.

This detector will demonstrate the excellent capabilities of pixels for pattern recognition. However, we already foresee to install several pixel layers

in the inner tracking system of ATLAS, and a huge R&D effort is underway to solve several remaining problems, like analog readout and time stamping, radiation survival of the electronics and the detector, cooling and mechanical integration, within the thinnest possible structure. Some of these problems have already been provided with viable solutions, as demonstrated by the several RadHard readout matrices implanted in DMILL technology, designed at CPPM, and tested recently in beam, bonded to a detector.

Acknowledgements

It is a pleasure to thank Petr Sicho, from FZU, Prague, who spent several months (including some nights!) for the installation of the automatic wafer inspection machine, and for the production tests.

The two-metal process used for the detector modules was developped in collaboration with CSEM, Neufchatel (contact persons: A. Perret and P. Weiss), where all detector wafers are produced. We want to stress the great effort made by IBM-France, Corbeil, and Montpellier Technologies (contact persons: D. Parison and J.J. Ichaï) during the whole prototyping period, as well as for the scheduling of the production. Finally, we want to thank the DELPHI collaboration, and in particular J.E. Augustin, for their support during the developpment of this project.

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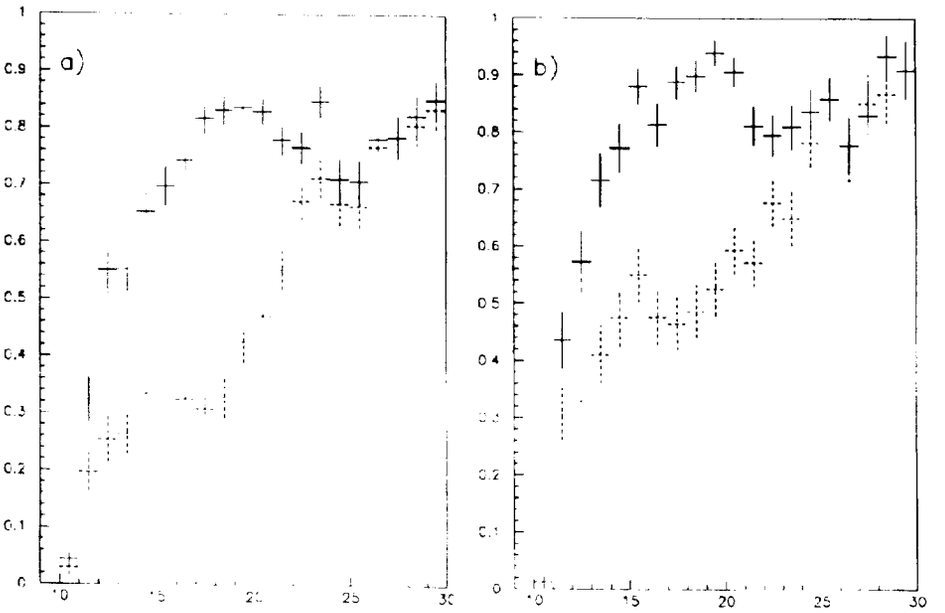

Figure 1: Track reconstruction efficiency vs. angle, with (solid crosses) and without (dashed crosses) the VFT, for jets with $p < 4\ GeV$ (a) and $p > 4\ GeV$ (b).

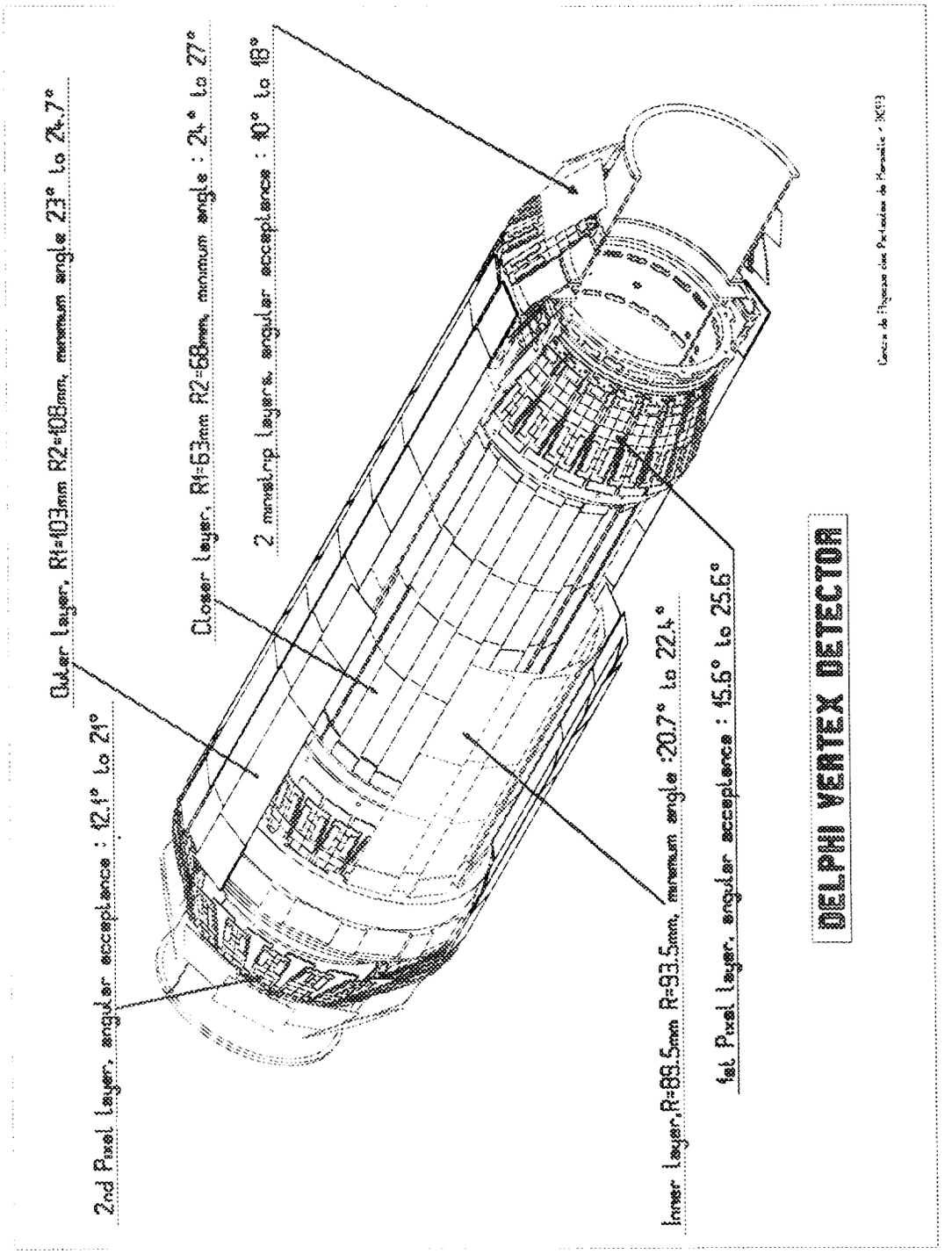

Figure 2: General layout of the Micro-vertex detector, equipped with the VFT.

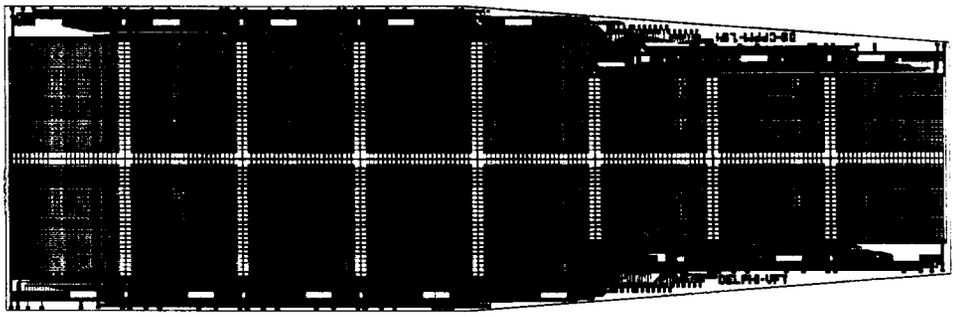

Figure 3: Layout of a detector module, showing the 2 different matrix sizes, and the buses.

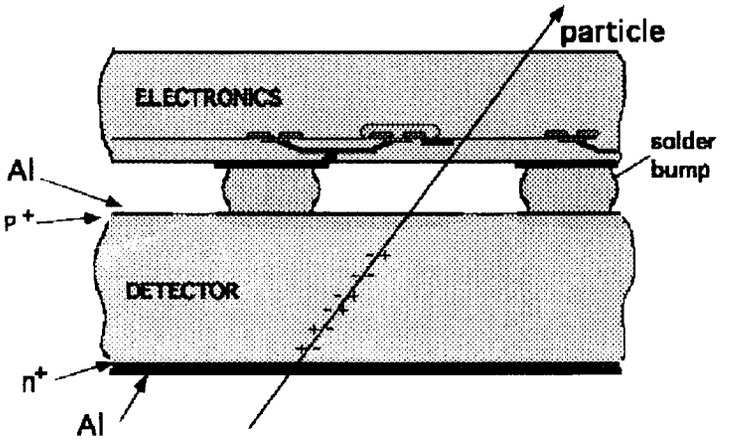

Figure 4: Principle of the hybrid pixel technique.

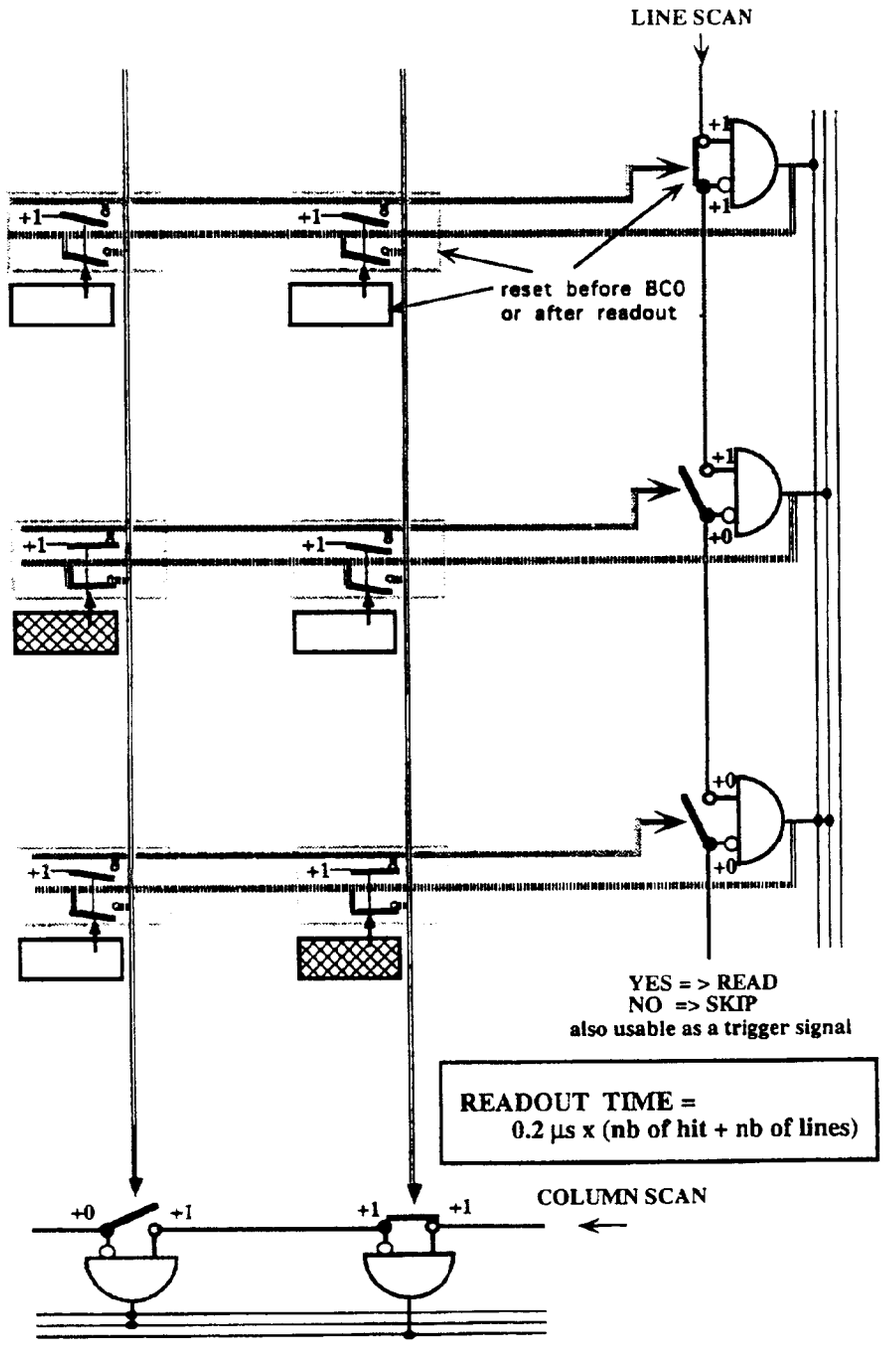

Figure 5: Sparse Data Scan Readout Diagram

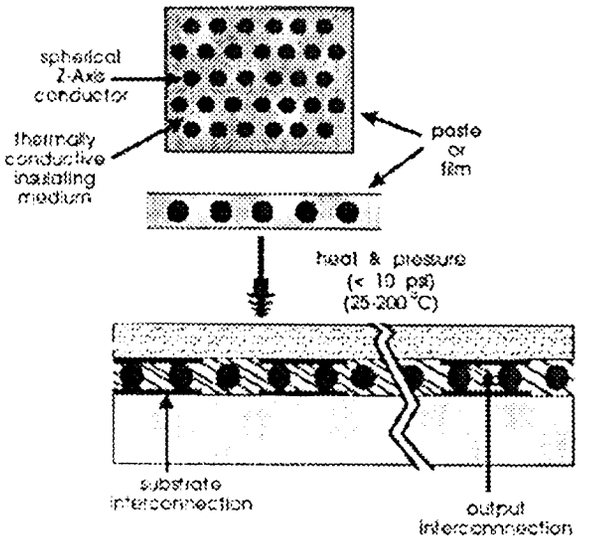

Figure 6: Principle of the Anisotropic Conductive Film technique.

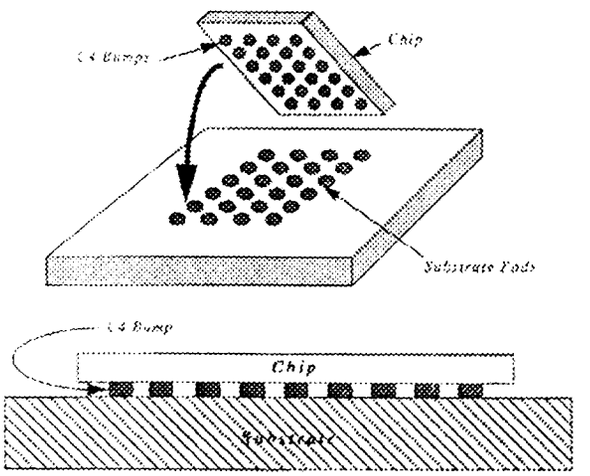

Figure 7: Principle of the Controlled Collapse Chip Connection, IBM.

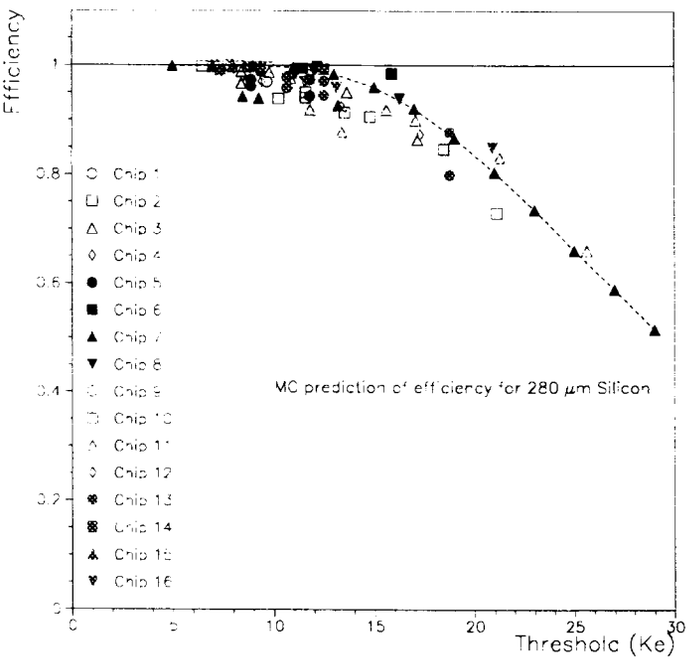

Figure 8: Efficiency curves as a function of threshold for the 16 electronic chips of a DELPHI pixel detector. The curve represents the Monte Carlo prediction at 40° incidence angle.

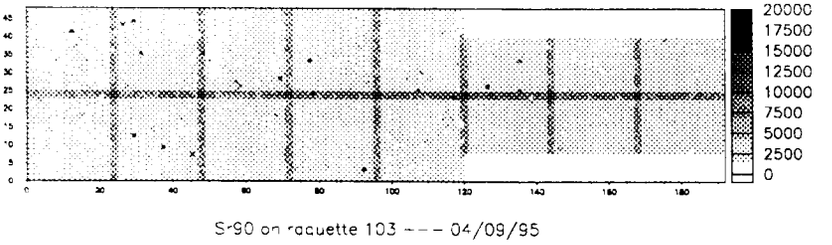

Figure 9: Counting uniformity using a ^{90}Sr source. Darker lines and columns represent the double size pixels at chip junction.

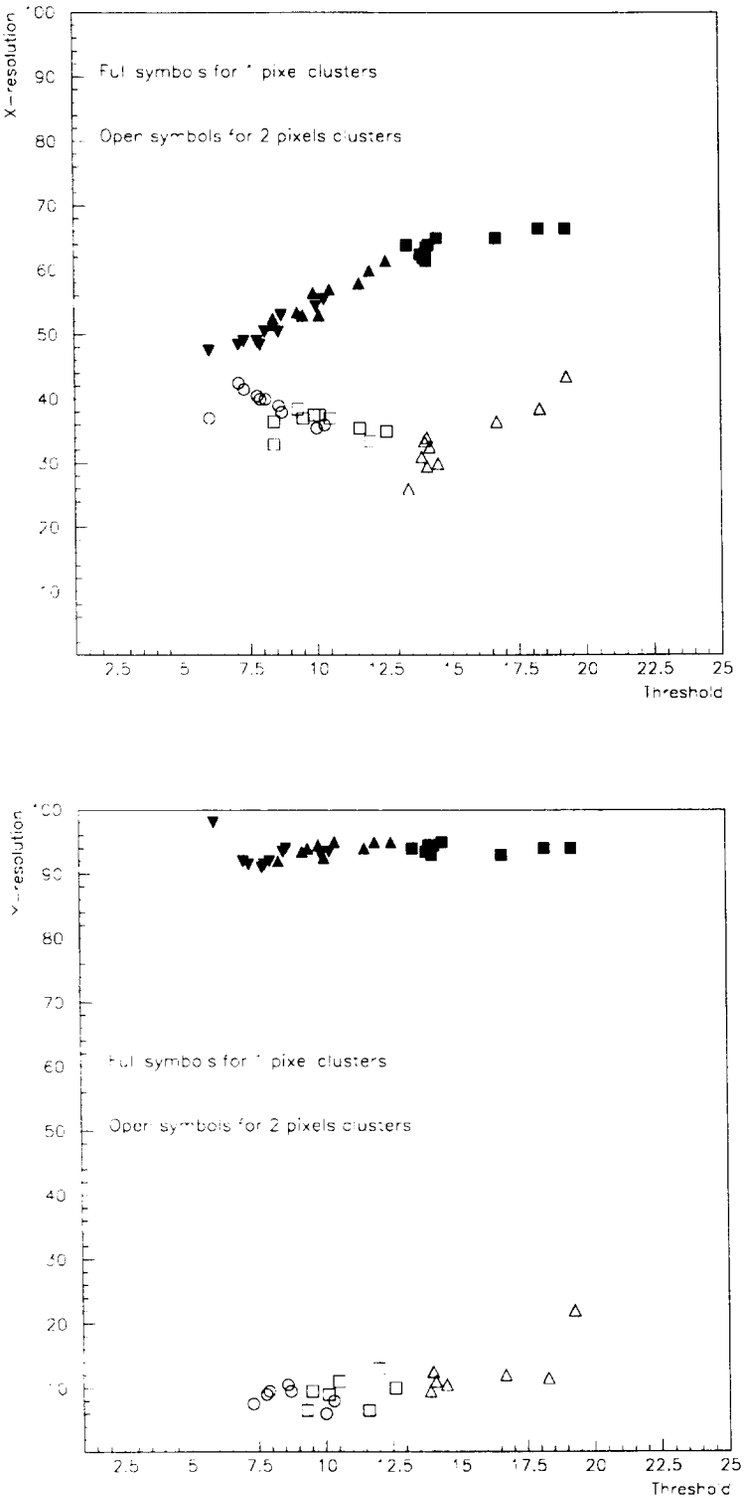

Figure 10: Resolution in the x and y direction, vs. adjusted threshold, in k.e$^-$.